

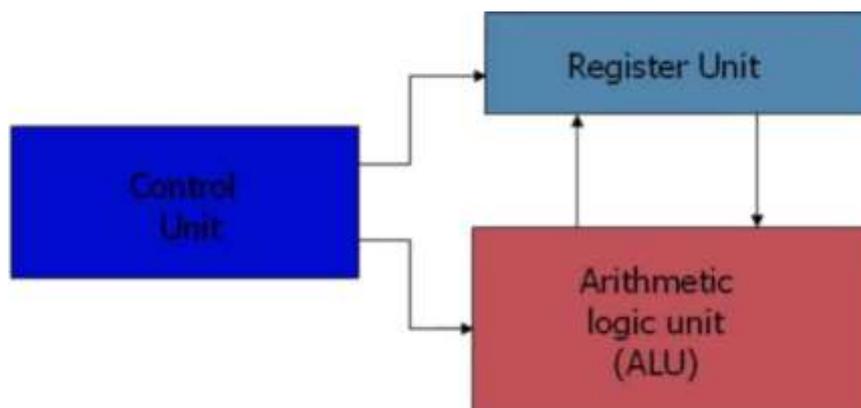
CPU Design

Central Processing Unit:

Its purpose is to

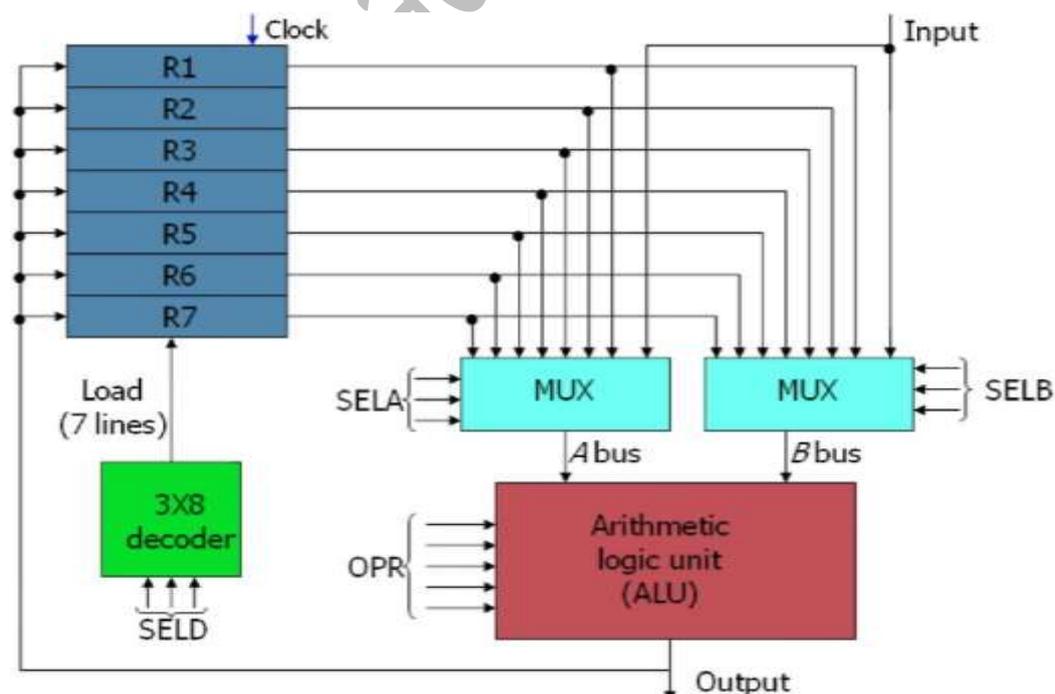
1. interpret instruction cycles received from memory and
2. perform arithmetic, logic and control operations with data stored in internal register, memory words and I/O interface units.

A CPU is usually divided into two parts namely processor unit (Register Unit and Arithmetic Logic Unit) and control unit.



Microprocessor and CPU organization

The processor unit consists of arithmetic unit, logic unit, a number of registers and internal buses that provides data path for transfer of information between register and arithmetic logic unit. The registers communicate each other not only for direct data transfer but also while performing various micro-operations.



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Reference: M Morris Mano, Computer System Architecture, Third Edition, Pearson Education

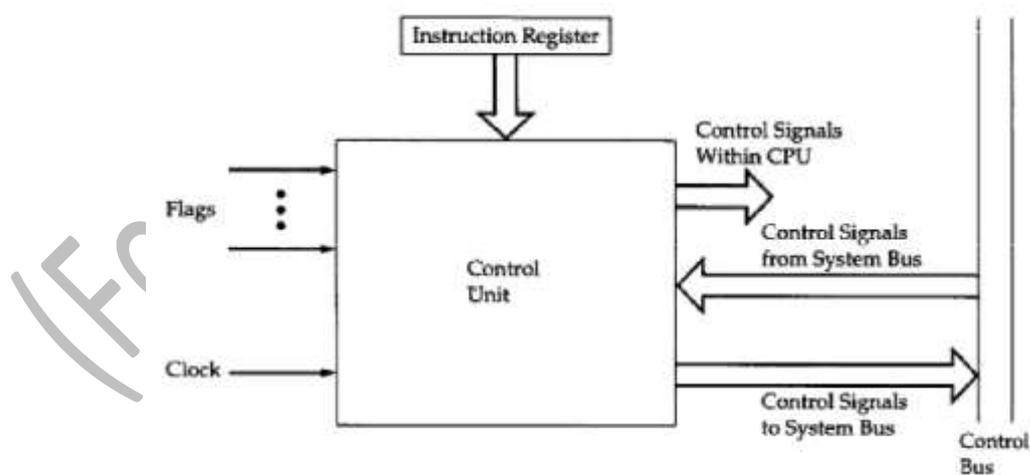
Note: For academic purpose only. For detailed explanation of contents please consult the above referred book

e.g. in the above diagram two sets of multiplexers select register which perform input data for ALU. A decoder selects destination register by enabling its load input. The function select in ALU determines the particular operation that to be performed.

Control Unit: It is the heart of CPU. It consists of a program counter, instruction register, timing and control logic. The control logic may be either hardwired or micro-programmed. If it is a hardwired, register decodes and a set of gates are connected to provide the logic that determines the action required to execute various instructions. A micro-programmed control unit uses a control memory to store micro instructions and a sequence to determine the order by which the instructions are read from control memory. It decoded the instruction and directs the necessary data to be moved from memory to ALU. It communicates both with ALU and main memory. It coordinates all activities of processor unit, peripheral devices and storage devices.

Design and implementation of CU includes

1. Defining basic elements of the processor
2. Describing micro-operations
3. Determine its function and how to perform microoperations.
4. Mechanism to
 - a. Know about state of the system (Input flags)
 - b. Control the behavior of the system.



The input to control unit are:

1. Flag: flags are headed to determine the status of processor and outcome of previous ALU operation.
2. Clock: All micro-operations are performed within each clock pulse. This clock pulse is also called as processor cycle time or clock cycle time.
3. Instruction Register: The opcode of instruction determines which micro-operation to perform during execution cycle.
4. Control signal from control bus: The control bus portion of system bus provides interrupt, acknowledgement signals to control unit.

The outputs from control unit are:

- Control signal within processor: These signals causes data transfer between registers, activate ALU functions.
- Control signal to control bus: These are signals to memory and I/O module. All these control signals are applied directly as binary inputs to individual logic gate.

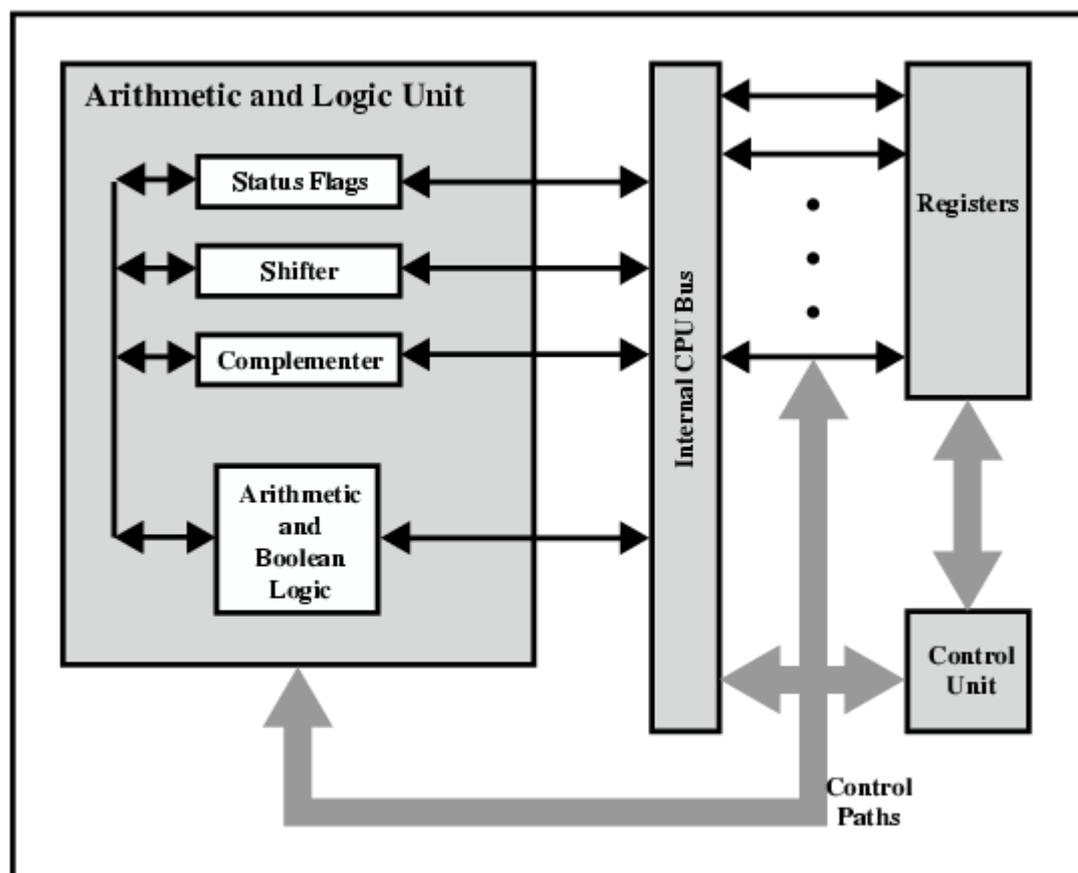
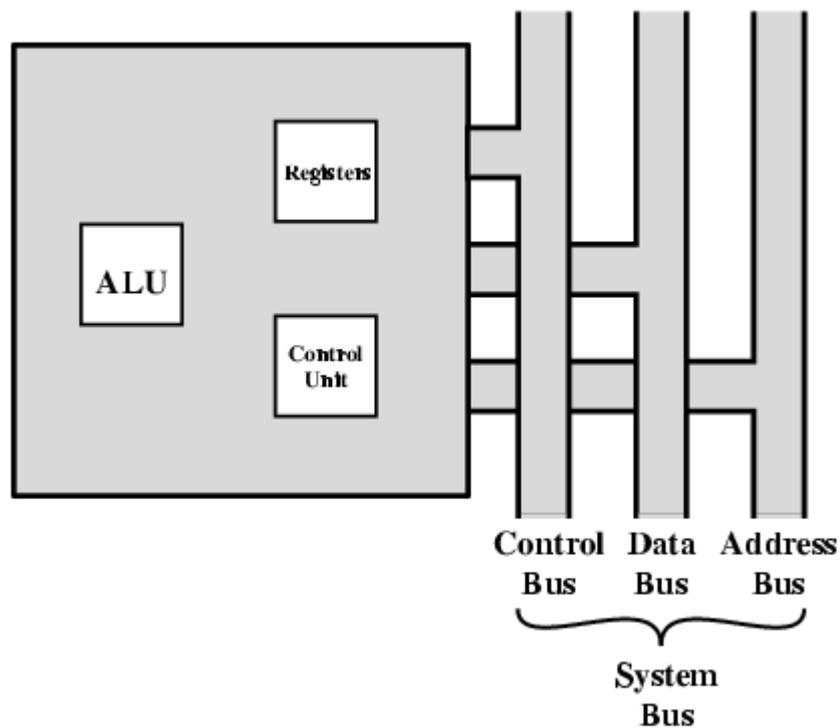


Figure 1: Internal Structure of CPU

CPU Functions

CPU Functions: Functions performed by the CPU include

1. Fetch & Interpret instructions.
2. Fetch, process and write the Data



Register Organization: Registers may be divided into two classes viz.

1. User-Visible Registers - enable the machine- or assembly-language programmer to minimize main-memory references by optimizing use of registers.
 - a. General Purpose registers
 - b. Data registers
 - c. Address registers
 - d. Segment pointers
 - e. Index registers
 - f. Stack Pointer

Design Issues:

- (i) General Purpose Vs Specialized purpose
 - (ii) Number of registers (8 to 32): RISC system may have 100s of register.
 - (iii) Register Length: Address register must hold largest address and data register the largest data type. Some machine allows contiguous registers to hold double length values.
 - (iv) Automatic or manual save.
2. Control and Status Registers - Used by the control unit to control the operation. They include
- a. PC (Program Counter)
 - b. IR (Instruction Register)
 - c. MAR (Memory Address Register)
 - d. MBR (Memory Buffer Register)
 - e. PSW (Program Status Word): With Sign, Zero, Carry, Equal, Overflow, Interrupt, Supervisor bits (status flags).

(For Academic Purpose)